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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/732,135	12/07/2000	Roshan J. Samuel	TI-31249	1005

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EXAMINER

DANG, KHANH NMN

ART UNIT	PAPER NUMBER
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2111

DATE MAILED: 01/13/2004

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/732,135

Applicant(s)

SAMUEL ET AL.

Examiner

Khanh Dang

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 11/03/2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-3, 5-7 and 9-11 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3, 5-7, and 9-11 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.
a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s) _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ 6) ☐ Other: _____

DETAILED ACTION

Claim Objections

Claim 5 is objected to because of the following informalities: In line 18, after "the bit," the word "at" should be changed to – as --. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-12 are rejected under 35 U.S.C. 102(e) as being anticipated by McCracken et al.

At the outset, it is noted that that similar claims will be grouped together to avoid repetition in explanation.

As broadly drafted, claims 1-12 do not define any structure that differs from McCracken et al. With regard to claims 1 and 3, McCracken et al. discloses a state

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machine input/output circuit responsive to a clock signal having cyclically repeating rising edges and falling edges, for providing data to an output port, comprising: a memory having a plurality of storage elements (DDR-SDRAM 16, 18, Fig. 1), each storage element having an input and an output, the input being programmably connectable to processor (col. 1, lines 13-20), for selection of data for storage therein; a first multiplexer (MUX 104) having an output (116, Fig. 3, for example), having a plurality of inputs (See at least Fig. 1) receiving the outputs of the memory, and a control input for receiving a control signal (106) generated by a control signal generator for controlling the first multiplexer (MUX 104) to select the first multiplexer inputs; and a clock edge selector circuit (44, Fig. 4, for example) for providing, in response to an edge select signal, the output of the first multiplexer (MUX 104) to the output port selectably on either the rising edges or the falling edges of the clock signal. With regard to claim 2, the clock edge selector circuit comprises the input of first and second flip-flops (176, 174) coupled to the output of the multiplexer, the first flip-flop changing states on said rising edge of clock pulse and said second flip-flop changing states on the falling edge of clock pulse; output of the first and second flip-flops (176, 174) coupled to first and second inputs of a second multiplexer (180); the control input (195) of the second multiplexer (180) coupled to the output of an edge select register; and the output of said second multiplexer coupled to the output port. With regard to claim 4, it is clear from the programmable logic and circuit configurations disclosed by McCracken et al. that they are programmable without any prior knowledge of the application device being controlled. With regard to claims 5-12, it is first noted that the words "first," "second,"

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and "third" used liberally and interchangeably by the Applicant to recite different flip-flops and MUXs depending on each drafted independent claim. Therefore, attention should be directed to flips-flops and MUXs of McCracken et al. based on their own characteristics/configurations (explained above), and "first," "second," or "third" should be assigned to them accordingly. For example, Flip-flop (202) is now readable as a "first flip-flop" recited in claim 5, the remaining flip-flops of Mc Mccracken et al. are readable as "first" or "second" flip-flop according to its own characteristic/configuration as already explained above. And similarly, in claim 6, MUX (188) is readable as a "third multiplexer." Other claims, as explained and in view of the above, are readily readable on Mccracken et al.

Response to Arguments

Applicants' arguments filed 11/03/2003 have been fully considered but they are not persuasive.

At the outset, Applicants are reminded that claims subject to examination will be given their broadest reasonable interpretation consistent with the specification. *In re Yamamoto*, 740 F.2d 1569, 1571, 222 USPQ 934, 936 (Fed. Cir. 1984). Applicants are also reminded that claimed subject matter not the specification, is the measure of the invention. Disclosure contained in the specification can not be read into the claims for the purpose of avoiding the prior art. *In re Sporck*, 55 CCPA 743, 386 F.2d, 155 USPQ 687 (1986).

With this in mind, the discussion will focus on how the terms and relationships thereof in the claims are met by the references. Response to any limitations that are not in the claims or any arguments that are irrelevant and/or do not relate to any specific claimed language will not be warranted.

With regard to claim 1 (with claims 2 and 3 stand or fall together), Applicants argued that McCracken et al. does not disclose “a plurality of storage elements, each storage element being adapted to store a bit and provide the bit as an output of said memory.” In response, it is first noted that it has been held that the recitation that an element is “adapted to” perform a function is not a positive limitation but only requires the ability to so perform. It does not constitute a limitation in any patentable sense. *In re Hutchison*, 69 USPQ 138. In any event, the memory used in McCracken et al. is DDR-SDRAM. All SDRAM comprise memory chips including the memory cells or a so-called “a plurality of storage elements.” Each cell stores a single bit, has a unique address that is defined by the intersection of a row and column, and provides the bit as an output of the memory. Applicants also argued that McCracken does not disclose a “first multiplexer ... having a plurality of inputs receiving the outputs of said memory.” Contrary to Applicants’ argument, McCracken et al. discloses a first multiplexer (MUX 104) having an output (116, Fig. 3, for example), having a plurality of inputs (See at least Fig. 1) receiving the outputs of the memory. With regard to claim 5 (with claims 6 and 7 stand or fall together), Applicants argued that McCracken et al. does not disclose “a memory having a plurality of storage elements, each storage elements being adapted to store a bit and provide the bit at [sic] a memory output of said memory, said memory

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outputs being connected to the inputs of said second multiplexer." In response, it is first noted that it has been held that the recitation that an element is "adapted to" perform a function is not a positive limitation but only requires the ability to so perform. It does not constitute a limitation in any patentable sense. *In re Hutchison*, 69 USPQ 138. In any event, the memory used in McCracken et al. is DDR-SDRAM. All SDRAM comprise memory chips including the memory cells or a so-called "a plurality of storage elements." Each cell stores a single bit, has a unique address that is defined by the intersection of a row and column, and provides the bit as an output of the memory. McCracken et al. also discloses a multiplexer (MUX 104) having an output (116, Fig. 3, for example), having a plurality of inputs (See at least Fig. 1) receiving the outputs of the memory. Note that the words first," "second," and "third" are used liberally and interchangeably by the Applicants to recite different flip-flops and MUXs depending on each drafted independent claim. Therefore, attention should be directed to flips-flops and MUXs of McCracken et al. based on their own characteristics/configurations as explained above, and "first," "second," or "third" should be assigned to them accordingly. With regard to claim 9 (with claims 10 and 11 stand or fall together), Applicants argued that McCracken et al. does not disclose "a memory having a plurality of storage elements, each storage elements being capable of storing a bit and provide the bit at [sic] a memory output of said memory." In response, it is first noted that it has been held that the recitation that an element is "capable of" performing a function is not a positive limitation but only requires the ability to so perform. It does not constitute a limitation in any patentable sense. *In re Hutchison*, 69 USPQ 138. In any event, the memory used in

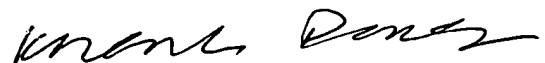
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McCracken et al. is DDR-SDRAM. All SDRAM comprise memory chips including the memory cells or a so-called "a plurality of storage elements." Each cell stores a single bit, has a unique address that is defined by the intersection of a row and column, and provides the bit as an output of the memory.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Any inquiry concerning this communication should be directed to Khanh Dang at telephone number 703-308-0211.



Khanh Dang
Primary Examiner